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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/656,985	09/07/2000	Anthony M. Chiu	00-C-015	2236

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/656,985	Applicant(s) CHIU, ANTHONY M.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *8-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6, line 6 cites: "mounting the integrated circuits in contact with each other".

However, the description in the specification (page 7, line 30; page 9, line 3; page 12, lines 2-4) and Figures 1 and 4 show the sensor segments/packages (104a, 104b, /402a, 402b, etc.) being spaced by a kerf/saw width.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamawaki et al (US Pat. 4894707) in view of Weiblen et al (US Pat. 6300169), Kunii et al (US Pat. 6252252) and further in view of Yoshihara et al (US Pat. 6255741) and Chan et al (US Pat. 6171879).

Regarding claims 1-4, Yamawaki et al disclose a method of forming an image/photo sensor comprising:

- an integrated circuit/photosensor chip (1 in Fig. 5f) having a portion remaining exposed after packaging/encapsulating
- a plurality of conventional leads (6 in Fig. 5f) adapted for further mounting/soldering, the packaging method further comprising:
- affixing the IC chip/die to a lead frame (Fig. 5c; Col. 2, line 66)
- connecting the IC die/chip to selected portions of the lead frame with bond wires, (Fig. 5d; Col. 2, line 67)and
- encapsulating a portion of the lead frame and the die except for the exposed region where the exposed region of the die remains exposed to the external light, the encapsulating step comprising: mounting the lead frame, die and the bond wires in a mold (21/22 in Fig. 5e) with a portion of the mold in contact with the exposed region of the IC die to prevent the encapsulating material from adhering to the exposed region of the IC die (Fig. 5e; Col. 3, line 50)

(Fig. 5f; Fig. 5a-e; Col. 2, line 50- Col. 3, line 50).

Yamawaki et al fail to specify using a linear array of photosensor IC being adapted for soldering the respective leads to a circuit board.

However, it is conventional in chip/leadframe packaging technology art to use the substrates such as lead frame, circuit board, etc. where a plurality of IC/an array are

wire bonded and subsequently being soldered to a circuit board to improve the cycle time and production yield.

Weiblen et al teach using a linear array of ICs (2 in Fig. 1) wire bonded on a conventional lead frame (Col. 2).

Kunii et al teach using a conventional circuit board where the leads of a plurality/array of optical IC devices are soldered to a circuit board (48 in Fig. 9; Col. 12, line 3). Kunii et al further teach using a variety of mold configurations including a mold cavity structure such that one surface of the mold cavity is a sloped surface receiving bond wires when the lead frame with the IC die is mounted in the mold (Fig. 14; Col. 12, line 51).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a linear array of photosensors being adapted for soldering the respective leads to a circuit board and a step of mounting the lead frame and die such that one surface of the mold cavity is a sloped surface receiving bond wires to improve the optical reflection, cycle time and production yield using Weiblen et al and Kunii et al's processes in Yamawaki et al's method.

Regarding claim 5, Yamawaki et al in view of Weiblen et al and Kunii et al fail to specify the separation distance between the mounted dice being equal to a kerf width for a singulation saw used in separating the packaged ICs.

It is a matter of a design choice in chip packaging and encapsulation technology art to select the dimensions such as kerf spacing, encapsulation width/length, saw/blade thickness, etc. to achieve the desired package dimensions.

Yoshihara et al teach using a saw where the width of the saw is slightly smaller than the kerf spacing/width of the devices (Fig. 12; Col. 9, line 3).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the separation distance between the mounted dice being equal to a kerf width for a singulation saw used in separating the packaged devices to reduce overall package dimensions and weight using Yoshihara et al's teaching in Yamawaki et al's method in view of Weiblen et al and Kunii et al.

Regarding claim 7, Yamawaki et al in view of Weiblen et al and Kunii et al fail to specify the step of soldering where the leads on the other side of soldered leads are being in floating contact with the conductive structures on the board to facilitate adjustment and removal of the ICs.

Chan et al teach using conventional floating contacts (26/26' in Fig. 2-5) with conductive layers/structure on the substrate to improve flexibility in connection and reduce stress/strain in an integrated sensor device (Col. 5, line 10- Col. 6, line 43).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a step of soldering where the leads on the other side of soldered leads are being in floating contact with the conductive structures

on the board to facilitate adjustment and removal of the IC Chan et al's teaching in Yamawaki et al's method in view of Weiblen et al and Kunii et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
05-02-02

Steven Loke
Primary Examiner

Steven Loke